Atomic Layer Deposition

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Growth of crystals and epitaxial structures, 12.04.2023

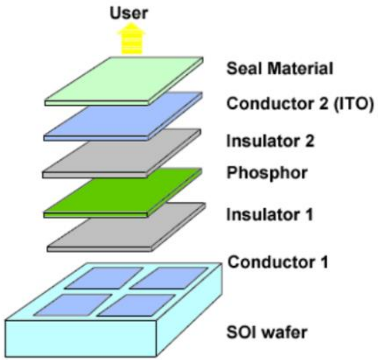
Outline

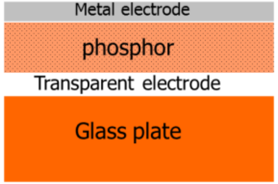
- ✓ Atomic Layer Deposition – a little old and new history
- ✓ Introduction to ALD (process principles, advantages/disadvantages)
- ✓ Experimental issues – process optimization, type of reactors
- ✓ Examples - semiconducting (ZnO, ZnSe) and dielectric (Al_2O_3, HfO_2) films
- ✓ Applications
- ✓ Summary

ALD - history

- ✓ Invented in 1977 by Suntola (Finland) for large area Thin Films Electroluminescent (TFEL) displays
- ✓ Previously called Atomic Layer Epitaxy (ALE)
- ✓ Used for monocrystalline, polycrystalline and amorphous films growth (III-V and II-VI compounds like ZnS and ZnSe)

T. Suntola and J. Antson, US Patent 4 058 430 (1977)





The word's first EL billboard Canada

Thin Films Electroluminescent (TFEL) displays

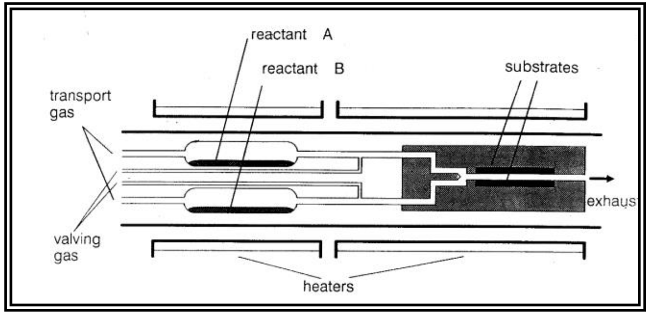
- Thin Films Electroluminescent (TFEL) Displays – origin in 1910, but commercially viable in 1980s
- Mechanism – radiative recombination of electrons or holes, which are separated as a result of doping to form a p-n junction (LED) or through excitation by impact of high energy electrons accelerated by strong electric field (phosphors)
- TFEL displays – particularly useful in applications where speed, brightness, high contrast, and a wide angle of vision is needed

ALD - history

F-120, first ALD reactor

ALD process – sequential deposition based on chemical reaction in mono-molecular adsorption layer

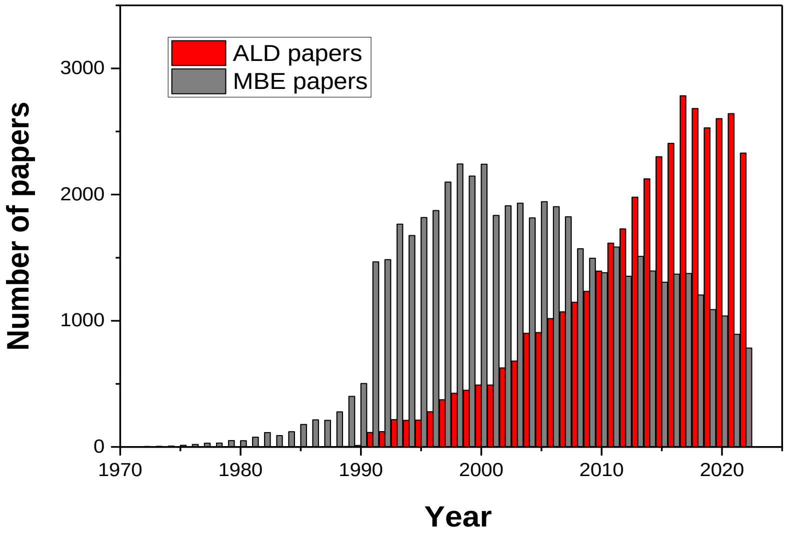
… → precursor A → purging → precursor B → purging→ precursor A → purging→ precursor B → purging → ….



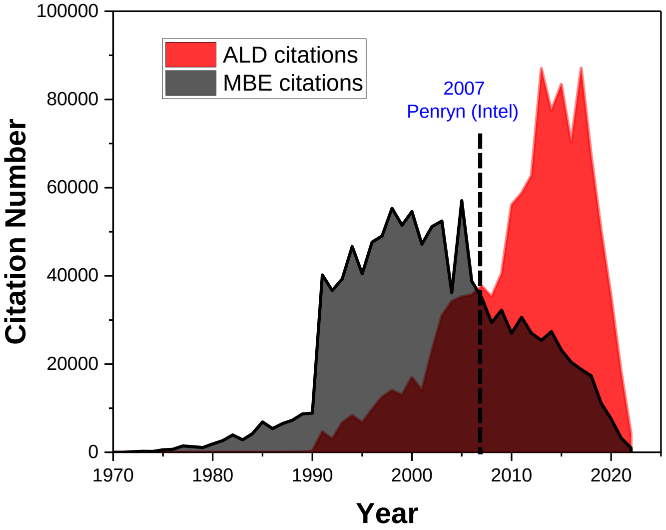
ALD technology in the 90s

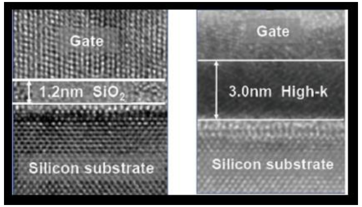
- ✓ III-V and II-VI compounds like ZnS and ZnSe
- ✓ inorganic precursors, often elemental
- ✓ relatively high growth temperature (350-450°C)

ALD and MBE – number of papers and citations



source: Web of Science

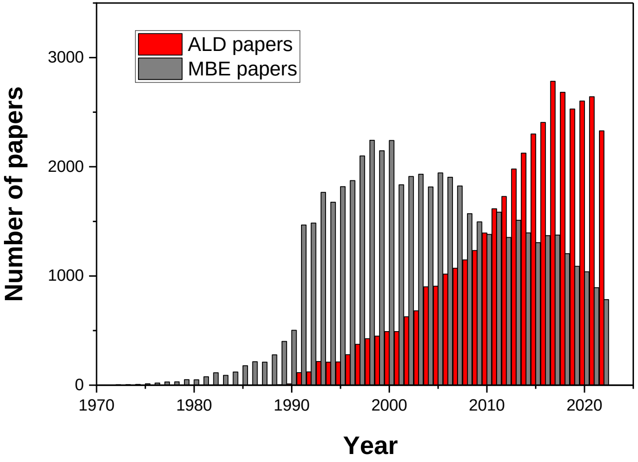


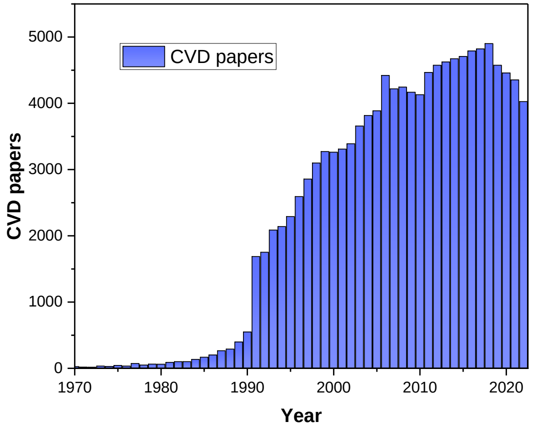


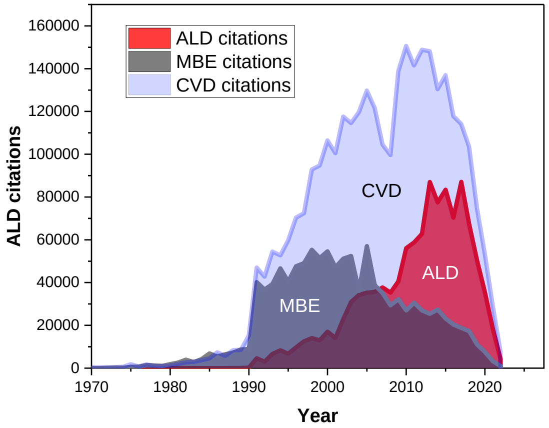
Breakthrough:

In 2007 Intel announced that their 45 nm generation processors include **a high-k HfO_2 gate dielectric made by Atomic Layer Deposition**

ALD, MBE and CVD – number of papers and citations



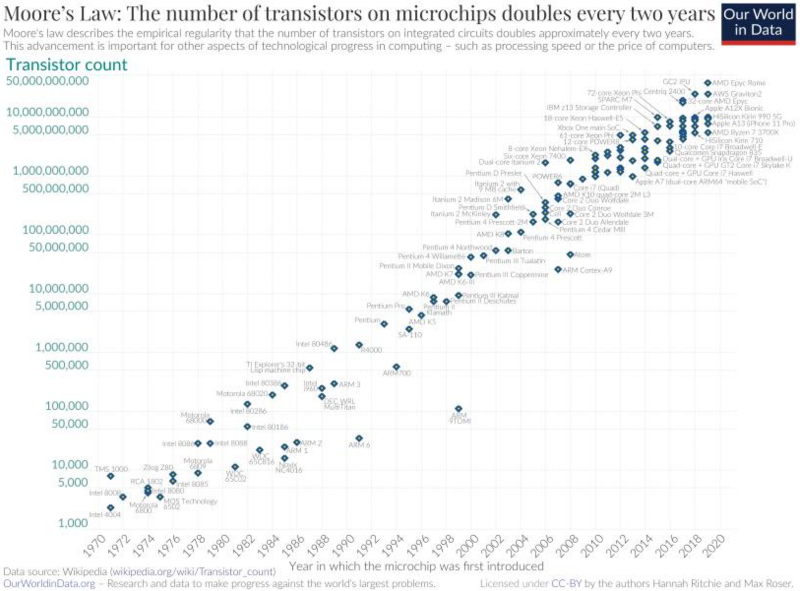


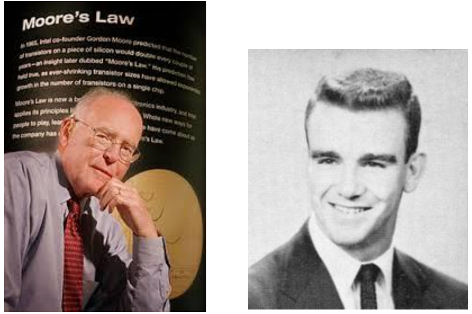


CVD – the main technology used in the industry

Moore’s Law

miniaturization in electronics





Gordon Moore (1929)
Co-founder of **Intel Corporation**

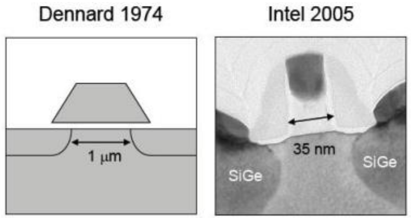
Paper „*Cramming more components onto integrated circuits*” (Electronics Magazine, 1965) – predicted personal computers and mobile technology

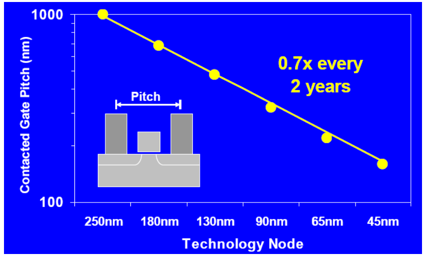
www. wikipedia.org

Number of transistors in one integrated circuit will be doubled every 18-24 months (quicker and cheaper computers)

Moore’s Law

miniaturization in electronics





http://electronics360.globalspec.com/article/5417/how-moore-s-law

Number of transistors in one integrated circuit:

Processor	Year	No transistors
4004(first Intel chip)	1971	2300
8086	1978	29 000
286	1982	134 000
Intel486	1989	1 200 000
Pentium III	1999	9 500 000
Pentium 4	2000	42 000 000
Penryn	2007	410 000 000

Technologies:

Processor	Year	Technology
Pentium	1993	800 nm
Pentium III	1999	250 nm
Pentium 4	2002	130 nm
Pentium D	2005	90 nm
Core 2 Duo	2006	65 nm
Penryn (Core 2 Duo new generation)	2007	45 nm
Intel® Core™ i7-5775R Processor	2015	14 nm
Intel	2018	10 nm
AMD		7 nm

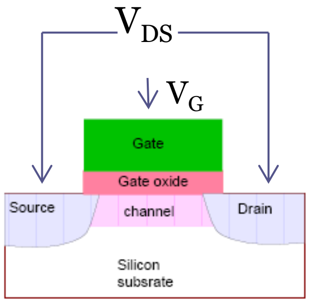
First transistor - 16 .12.1947
Bell Telephone Laboratories
Bardeen, Brattain & Shockley
Nobel Prize 1956

http://www.porticus.org/bell/belllabs_transistor.html)

First transistor radio (1954)
Based on 4 transistors...

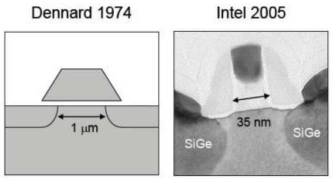
1 transistor in 1954 – 2.5$
2010 – more than million transistors = 1$

Miniaturization in electronics



MOSFET = Metal-Oxide Semiconductor Field-Effect Transistor

Si/SiO_2 technology



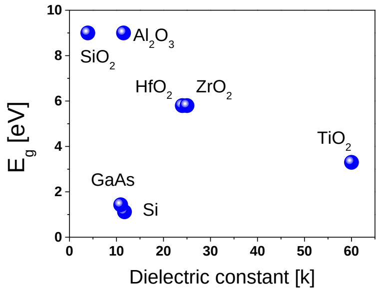
	1974	2005 65 nm node
Physical gate length:	> 1.0 µm	35 nm
Electrical channel length:	1.0 µm	< 20 nm
Gate oxide thickness:	**35 nm**	**1.2 nm**
Operating voltage:	4.0 V	1.2 V

Problems with gate leakage !

$$V = \frac{Qd}{\varepsilon A}$$

Low voltage + lower thickness
→ ε should be increased !

High-k gate oxides

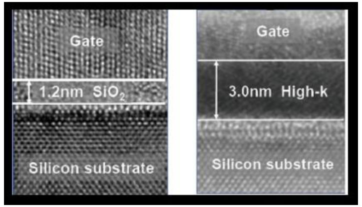


Problems with high-k oxides:

- ε value for thin films is usually lower than for the same bulk material
- to maintain high ε high-k oxide layer (ZrO_2, HfO_2) should be densely packed, uniform & with low defect density
- high-k oxide films deposited with conventional methods used in CMOS technology did not fulfilled the requirements…

Breakthrough:

In 2007 Intel announced that their 45 nm generation processors include **a high-k HfO_2 gate dielectric made by Atomic Layer Deposition (ALD)**



High-k dielectrics were introduced:

- improved gate coupling ratio
- reduced parasitic coupling
- smoother morphology (easier integration)

High-k oxides

- ✓ In 2007 Intel announced that their 45 nm generation processors include a high-k HfO_2 gate dielectric made by Atomic Layer Deposition (ALD)
- ✓ ALD guarantees flat, conformal, uniform films with reproducible thickness, low stress, uniform stoichiometry and low defect density
- ✓ A major driving force for the recent ALD interest is the prospective seen for ALD in scaling down microelectronic devices.
- ✓ SiO_2 replaced by HfO_2 – important consequences, because the main advantage of Si was native oxide SiO_2!
- ✓ Because of native oxide Si was used in electronics instead of Ge, which has better electrical properties (higher hole mobility)

Eddystone Receiver Model EC-10

Germanium based radio

„The biggest change in transistor technology in 40 years”
Gordon Moore

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ALD cycle

ZnO growth: DEZn + water

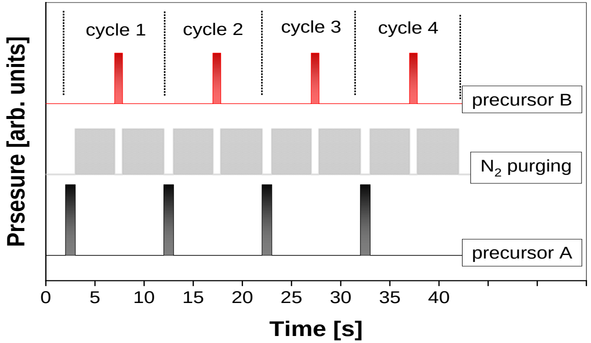
$$C_2H_5 - Zn - C_2H_5 + H_2O \rightarrow ZnO + 2\,C_2H_6$$

DEZn phase:

$$\text{surface} - OH + C_2H_5 - Zn - C_2H_5 \rightarrow \text{surface} - O - Zn - C_2H_5 + C_2H_6$$

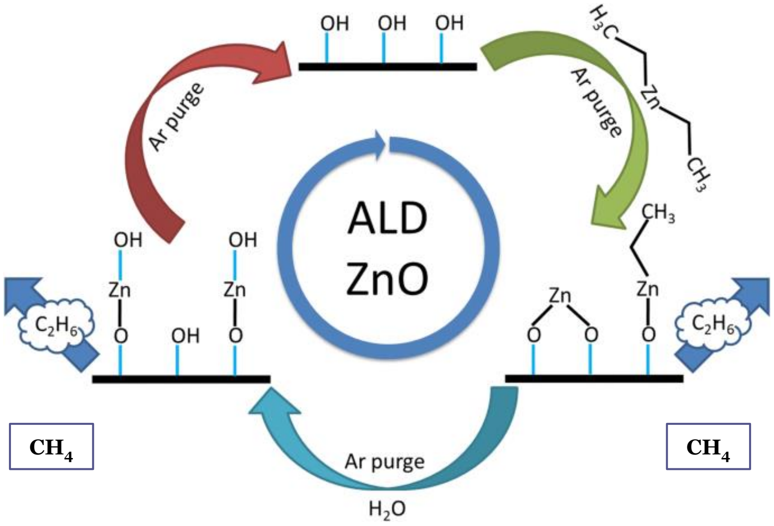
Water phase

$$\text{surface} - O - Zn - C_2H_5 + H_2O \rightarrow \text{surface} - O - Zn - OH + C_2H_6$$



ZnO growth: DMZn + water

$$CH_3 - Zn - CH_3 + H_2O \rightarrow ZnO + 2\,CH_4$$



ALD cycle

ALD → sequential growth process

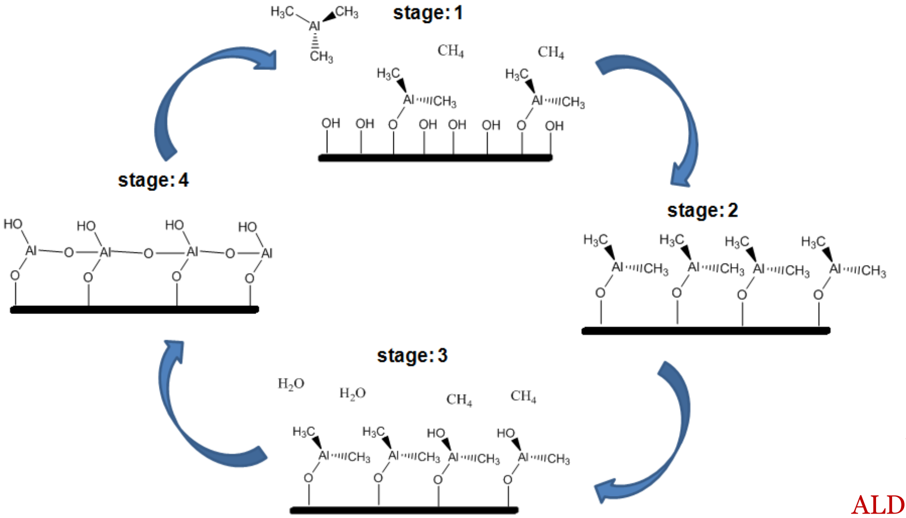
chemical **reaction between two reagents**

→ precursor 1→ purging → precursor 2→ purging →

$$2Al(CH_3)_3 + 3H_2O \rightarrow \mathbf{Al_2O_3} + 6CH_4$$

→TMA→ N_2→ H_2O→ N_2 →TMA→ N_2→ H_2O→ N_2 → TMA→ N_2→ H_2O→ N_2 →

$Al(CH_3)_3$ = TMA



Purging → removing excess precursor and reaction by-products

In the ideal ALD cycle only one monolayer (ML) of the deposited material is created. Thickness of the growing film is proportional to the number of cycles → very thin layers can be obtained repetitively and with high accuracy .

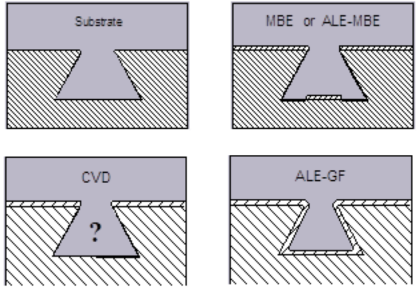
Usually in a real ALD process less than 1 ML/cycle is created (steric hindrance effect), but thickness always scales with a number of cycles.
Very slow growth process!

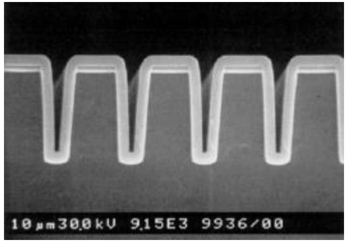
ALD guarantees flat, conformal, uniform films with reproducible thickness, low stress, uniform stoichiometry and low defect density

ALD → covering of developed surfaces

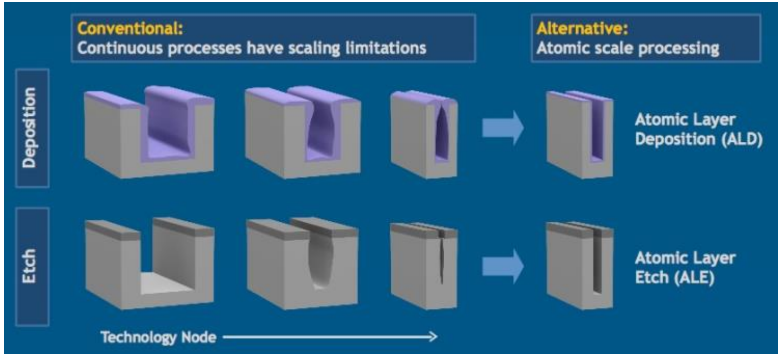
Self-limiting growth process leads to uniform covering of every surface, even with highly developed morphology (aspect ratio up to 100)

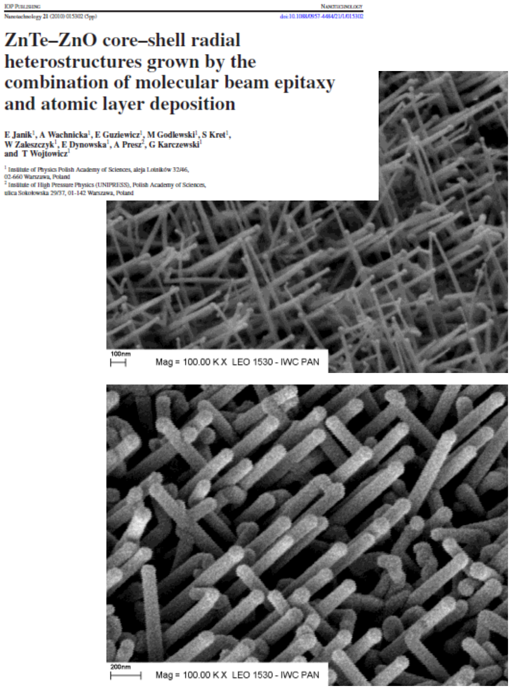
Aspect ratio = depth/diameter





Amorphous Al_2O_3 by ALD
University of Helsinki

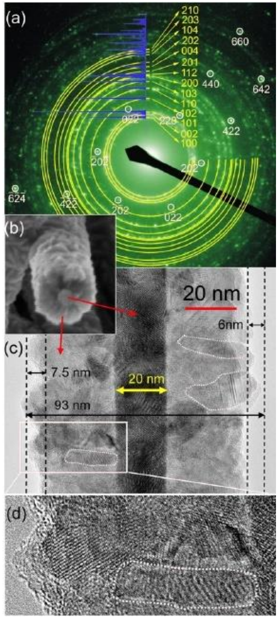



IOP Publishing   Nanotechnology
Nanotechnology 21 (2010) 015302 (5pp)   doi:10.1088/0957-4484/21/1/015302

ZnTe–ZnO core–shell radial heterostructures grown by the combination of molecular beam epitaxy and atomic layer deposition

E Janik[1], A Wachnicka[1], E Guziewicz[1], M Godlewski[1], S Kret[1], W Zaleszczyk[1], E Dynowska[1], A Presz[2], G Karczewski[1] and T Wojtowicz[1]

[1] Institute of Physics Polish Academy of Sciences, aleja Lotników 32/46, 02-660 Warszawa, Poland
[2] Institute of High Pressure Physics (UNIPRESS), Polish Academy of Sciences, ulica Sokołowska 29/37, 01-142 Warszawa, Poland



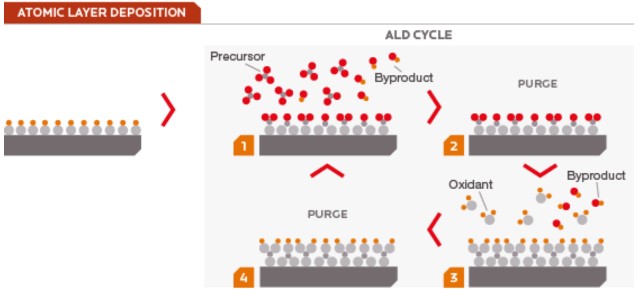
Atomic Layer Deposition vs Chemical Vapor Deposition

Both CVD and ALD are based on chemical **reaction between two reagents (precursors)**, but:

ALD → sequential process

→ precursor 1→ purging → precursor 2→ purging →

No reaction inside the chamber!

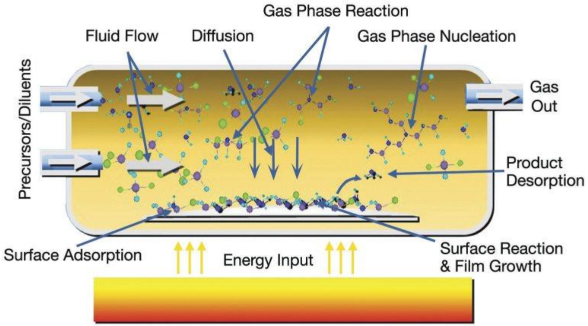


www.asm.com/technology/key-technologies/atomic-layer-deposition

Surface should be saturated during each half-reaction → growth is self-limiting, so its homogeneity does not depend on the constancy of the flow of reactants in space and time

CVD → continuous process

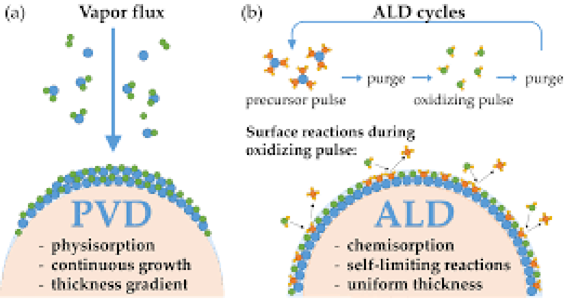
Reaction takes place inside the chamber!

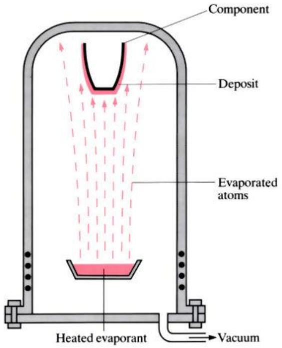


https://www.mksinst.com/n/cvd-physics

For homogeneous growth, the stream of reactants should be constant in space and time

Atomic Layer Deposition vs Physical Vapor Deposition





www.open.edu/openlearn/science-maths-technology/engineering-technology/manupedia/physical-vapour-deposition-pvd

PVD → based on physisorption ($T_G < T_{source}$); continuous growth, thickness gradient

ALD → based on chemisorption ($T_G > T_{precursor}$); self-limiting reactions, uniform growth

MBE, CVD, PVD → the growth is controlled by the flux of reagents

ALD → the growth is controlled by the surface of the growing film

J. Appl. Phys. 97, 121301 (2005)

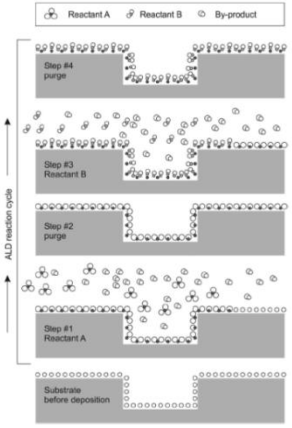
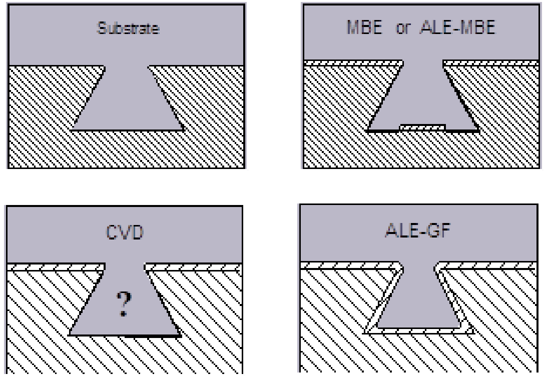
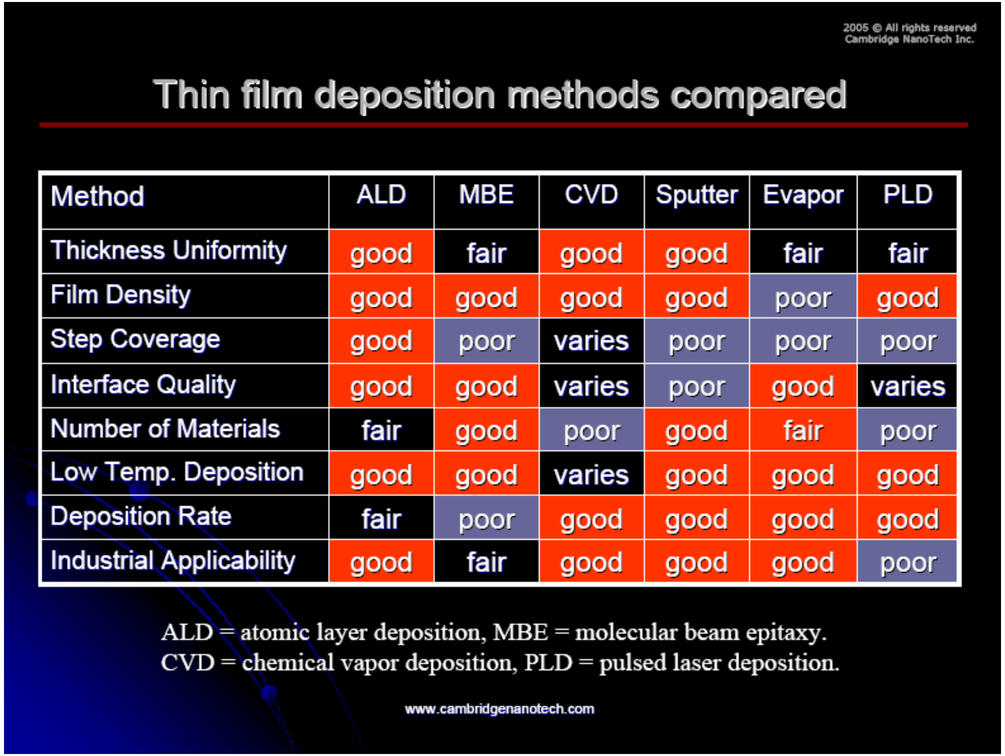


FIG. 2. Schematic illustration of one ALD reaction cycle.



Thin film deposition methods compared



Thin film deposition methods compared

Method	ALD	MBE	CVD	Sputter	Evapor	PLD
Thickness Uniformity	good	fair	good	good	fair	fair
Film Density	good	good	good	good	poor	good
Step Coverage	good	poor	varies	poor	poor	poor
Interface Quality	good	good	varies	poor	good	varies
Number of Materials	fair	good	poor	good	fair	poor
Low Temp. Deposition	good	good	varies	good	good	good
Deposition Rate	fair	poor	good	good	good	good
Industrial Applicability	good	fair	good	good	good	poor

ALD = atomic layer deposition, MBE = molecular beam epitaxy.
CVD = chemical vapor deposition, PLD = pulsed laser deposition.

www.cambridgenanotech.com

ALD guarantees flat, conformal, uniform films with reproducible thickness, low stress, uniform stoichiometry and low defect density

www.cambridgenanotech.com

Type of chemical reactions

- ✓ Synthesis → two elemental precursors
- ✓ Single exchange chemical reaction → elemental + chemical compound
- ✓ Double exchange chemical reaction → two compounds

Every kind of ALD process requires specific growth temperature and can provide material with different properties

ZnS

1) **Synthesis**
   precursors: zinc i sulphur:

$$Zn + ½ S_2 \rightarrow ZnS$$

2) **Single exchange**
   precursors: zinc Zn and hydrosulphide

$$Zn + H_2S \rightarrow ZnS + H_2$$

3) **Double exchange**
   precursors: zinc chloride $ZnCl_2$ and hydrogen sulfide H_2S

$$ZnCl_2 + H_2S \rightarrow ZnS + 2\ HCl$$

ZnO

1) Precursors: zinc chloride $ZnCl_2$ and H_2O (**double exchange**)

$$ZnCl_2 + H_2O \rightarrow ZnO + 2HCl$$

2) Precursors: zinc acetate $Zn(CH_3COO)_2$ and H_2O (**double exchange**)

$$Zn(CH_3COO)_2 + H_2O \rightarrow ZnO + 2CH_3COOH$$

3) dimethyl zinc $Zn(CH_3)_2$ and H_2O (**double exchange**)

$$Zn(CH_3)_2 + H_2O \rightarrow ZnO + 2CH_4$$

4) diethylzinc $Zn(C_2H_5)_2$ and H_2O (**double exchange**)

$$Zn(C_2H_5)_2 + H_2O \rightarrow ZnO + 2C_2H_6$$

5) zinc Zn and oxygen O (**synthesis**)

$$Zn + O \rightarrow ZnO$$

Type of chemical reactions and ALD window

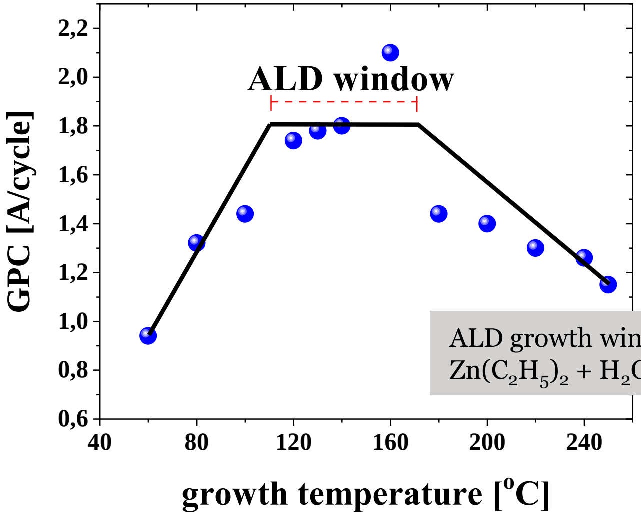
ZnO

$ZnCl_2 + H_2O$	430°C-500°C, epitaxial films
$Zn(CH_3COO)_2 + H_2O$	300°C-360°C, polycrystalline growth
$Zn(C_2H_5)_2 + H_2O$	60°C-300°C, epitaxial growth from 250°C
$Zn(CH_3)_2 + H_2O$	30°C-300°C, polycrystalline growth

ALD window → specific to the particular chemical exchange reaction

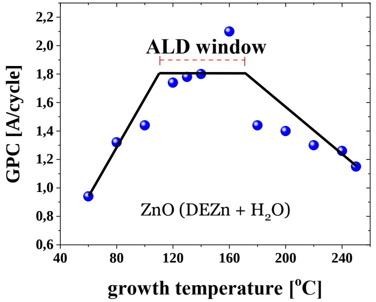
ALD growth window
→ GPC does not depend on growth temperature

GPC = Growth per Cycle

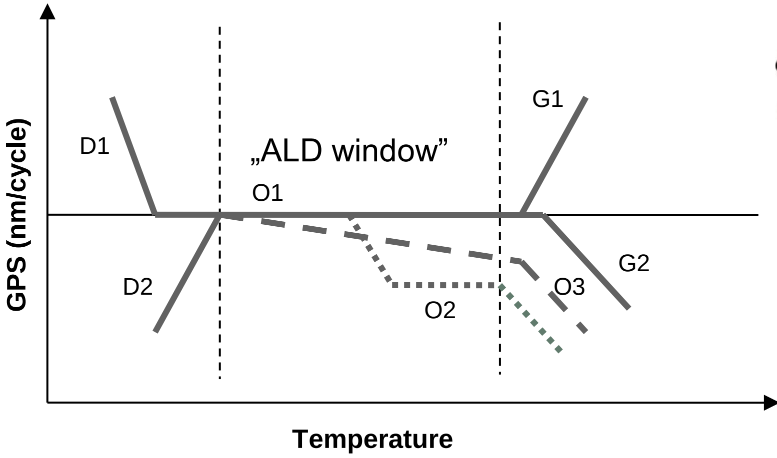


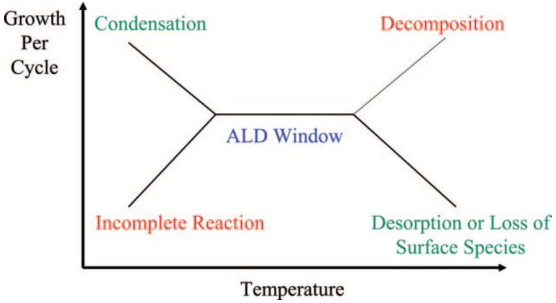
ALD growth window for ZnO:
$Zn(C_2H_5)_2 + H_2O \rightarrow ZnO + 2C_2H_6$

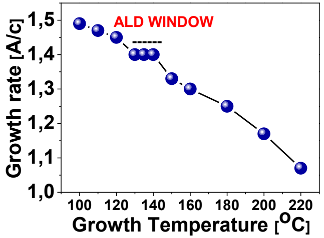
ALD window



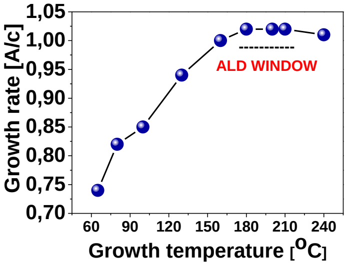
ZnO
ALD window: 100°C-160°C
GPC ~ 1.8 Å/c







HfO_2
ALD window: 130°C-140°C
GPC ~ 1.4 Å/c



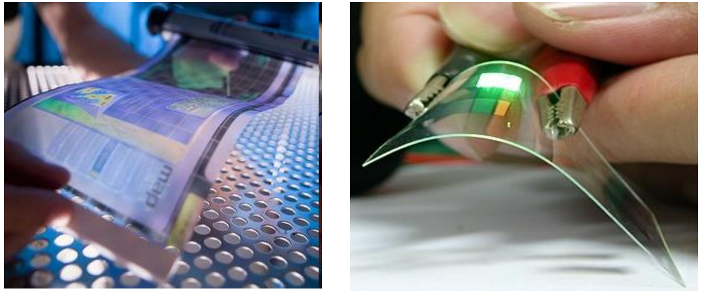
Al_2O_3
ALD window: 180°C-220°C
GPC ~ 1.0 Å/c

- ✓ D1 → volume condensation
- ✓ D2 → activation energy not reached
- ✓ O1 → perfect growth (1 ML/cycle)
- ✓ O2 → saturation of the surface reaction occurs with a partial monolayer
- ✓ O3 → saturation density decreases with increasing temperature (characteristic of non-oriented surfaces; polycrystalline or amorphous materials)
- ✓ G1 → volume condensation (reagent decomposes into non-volatile products)
- ✓ G2 → the layer formed is not very stable and evaporates

ALD → low deposition temperature

ALD → 100-300°C, CVD → 500-600°C

Organic electronics
hybrid organic-inorganic devices



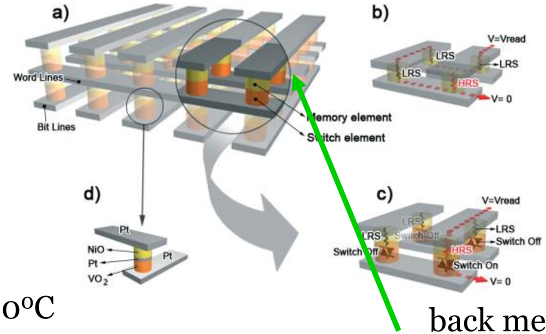
T‹ 200°C

- light weight, mechanically flexible, transparent, low costs
- new applications: smart windows, electronic paper, printed electronics, flexible display…

Organic electronics

- Low thermal & mechanical stability
- Low carrier mobility
- Inorganic partner needed; low temperature processing

3D memories
Back End Of Line (BEOL) technology



T‹ 350°C

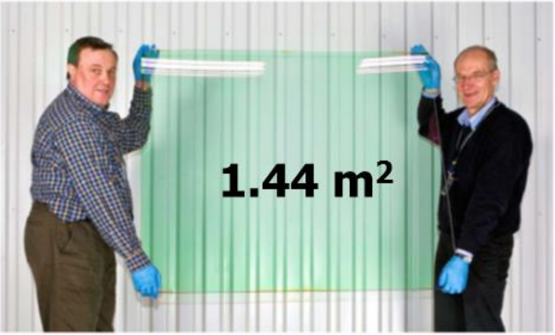
back metallization

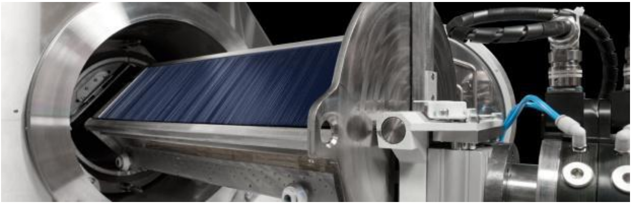
BEOL architecture (3 dimensional)→ bottom metallization semiconductor deposition and after dopant activation **after** metallization

IV group (Si, Ge) and III-V semiconductors excluded due to the high thermal budget

CMOS technology ~ up to **1000°C**

ALD → possible deposition on large substrates





Solar cells applications!

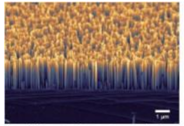


Figure 1. Scanning electron micrograph of wet-chemically etched silicon nanowires.
(Source: Max Planck Institute for the Science of Light)

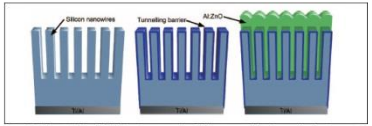


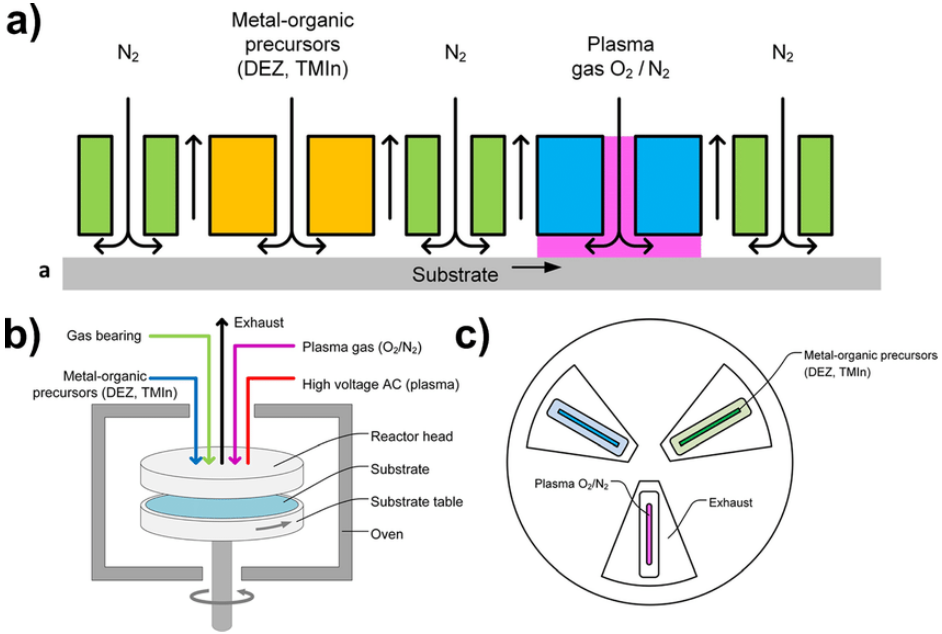
Figure 2. Schematic of the SIS fabrication process: The SiNWs are coated by the tunneling barrier material and subsequently by the AZO contact layer. (Source: Max Planck Institute for the Science of Light)

sitn.hms.harvard.edu

Commercial ALD reactors

ALD reactors P400, Planar Systems

Special ALD reactors



www.researchgate.net/figure/Color-online-a-Schematic-drawing-of-the-spatial-ALD-concept

Outline

- Atomic Layer Deposition – a little old and new history
- Introduction to ALD (process principles, advantages/disadvantages)
- Experimental issues – process optimization, type of reactors
- Examples - semiconducting (ZnO, ZnSe) and dielectric (Al_2O_3, HfO_2) films
- Applications
- Summary

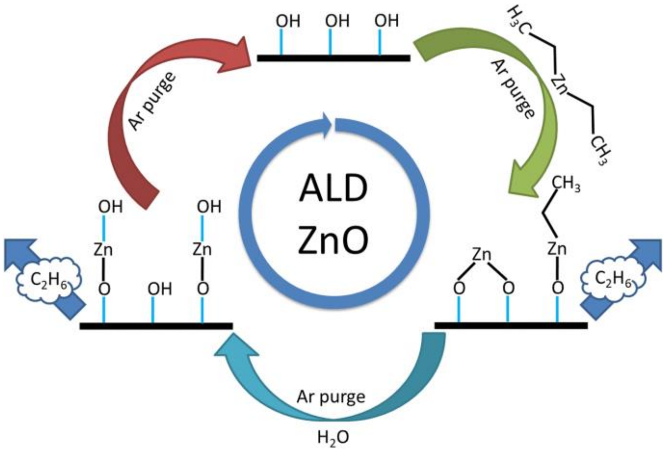
ALD process modeling

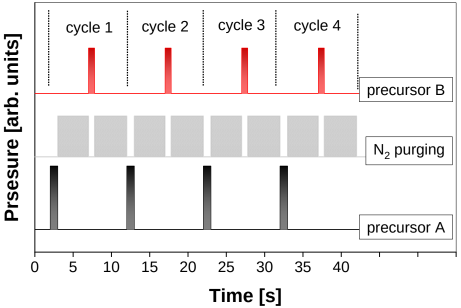
$Zn(C_2H_5)_2 + H_2O \rightarrow ZnO + 2C_2H_6$

- ✓ DEZn pulsing time
- ✓ DEZn purging time
- ✓ Water pulsing time
- ✓ Water purging time
- ✓ Growth temperature
- ✓ Precursor's temperature

~ 20^5 possibilities !

ALD cycle





Point defects concentration exponentially increase with deposition temperature:

$$n(T) \cong N_0 e^{-E_D/k_B T}$$

E_D= 1 eV

T = 300K → 10^9
T= 1000K → $5 \cdot 10^{18}$

Low temperature growth limits point defects formation

Precursors doses (pulsing time)

The density of molecules in gas can be expressed as

$$\rho_N = \frac{p_R}{kT} \quad (m^{-3})$$

where p_R – partial pressure of the reagent in the source, k- Boltzmann constant, T – temperature

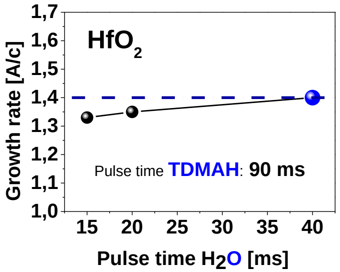
The required dose of reagent, N, can be expressed in terms of partial pressure and volume

$$\frac{p_R V}{kTu} = Aa_S$$

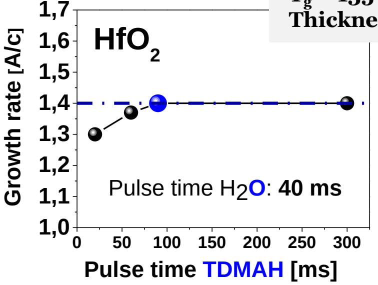
where V (m^3) is the volume of the gas dose containing the reactant at partial pressure p_R, A (m^2) –substrate area, a_S (molecules/m^2)– monolayer surface saturation density, u – material consumption factor (usually 0.1 – 0.8), or in a sense of reaction time and mass flow:

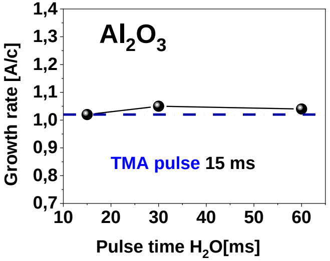
$$t = 2.23\times10^{-21}\frac{Aa_S}{Fu} \quad (s)$$

F – reagent mass flow
The typical saturation density of the monolayer surface ranges from 0.5×10^{19} till 1.5×10^{19} /m^2.

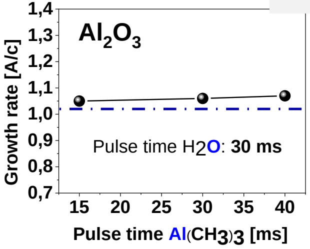


T_g = 135°C; T_{Hf} = 110°C
Thickness ~ 40 nm





T_g = 200°C; T_{Al} = RT
Thickness ~ 50 nm

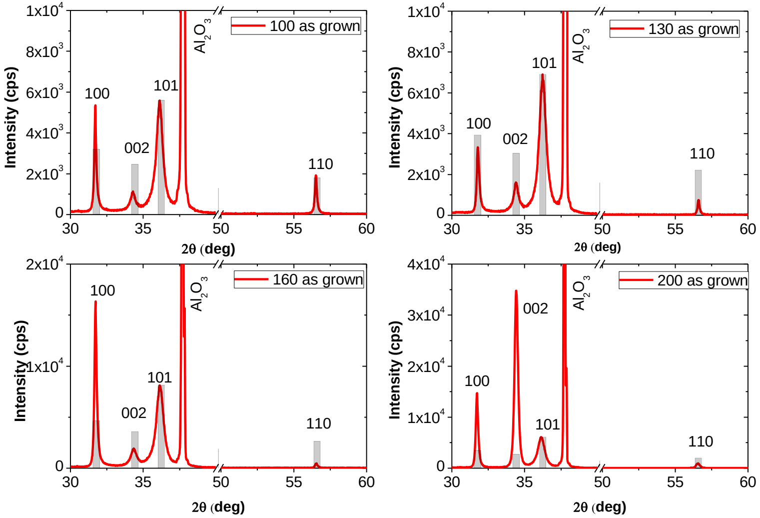


S. Gierałtowska, PhD thesis

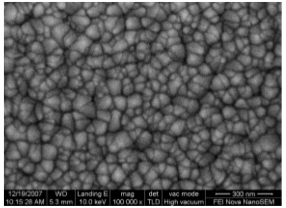
Growth temperature

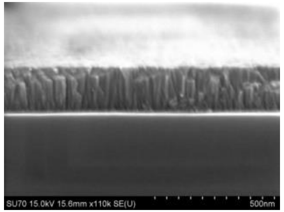
ZnO by ALD – structural properties

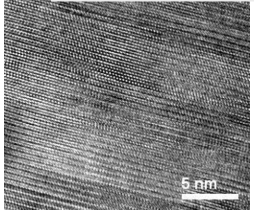
- T_G =100, 130, 160 and 200°C → polycrystalline films
- As grown and annealed films (O_2, RTP, 3 min., 800°C)
- Thickness ~ 900 nm (6.000 cycles)



E. Przezdziecka, E. Guziewicz, D. Jarosz, et al.,
J. Applied Physics (2021)

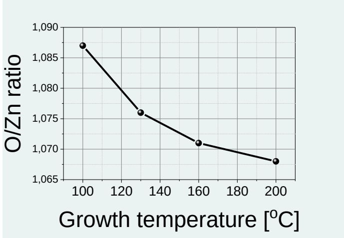


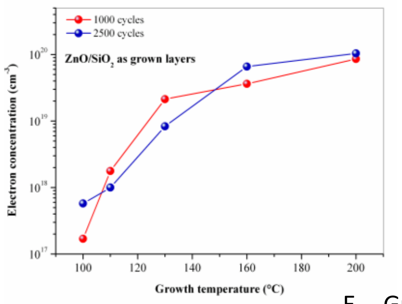


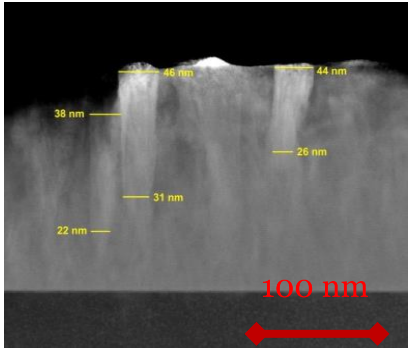


TEM measurements
Piotr Dłużewski, IF PAN

E. Guziewicz et al., **J. Appl. Phys. 103**, 033515 (2008)
T. Krajewski et al., **Microelectronics J. 40**, 293 (2009)





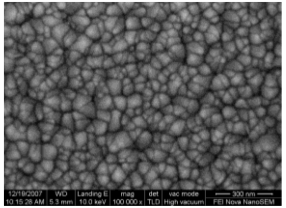


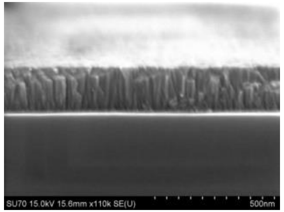
E. Guziewicz et al., **Semiconductor Science & Technology 27**, 074011 (2012)

ZnO by ALD – growth temperature

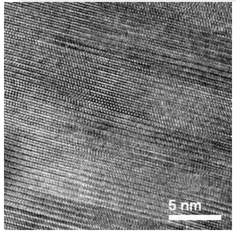
- T_G =100, 130, 160 and 200°C → polycrystalline films
- As grown and annealed films (O_2, RTP, 3 min., 800°C)
- Thickness ~ 900 nm (6.000 cycles)

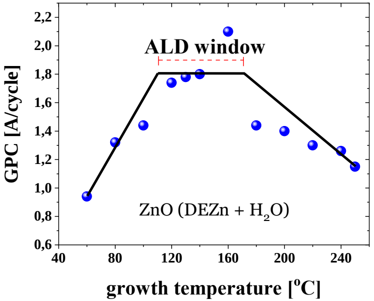
$Zn(C_2H_5)_2 + H_2O \rightarrow ZnO + 2C_2H_6$

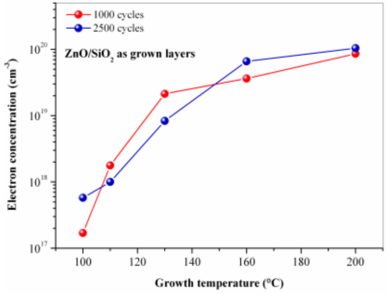




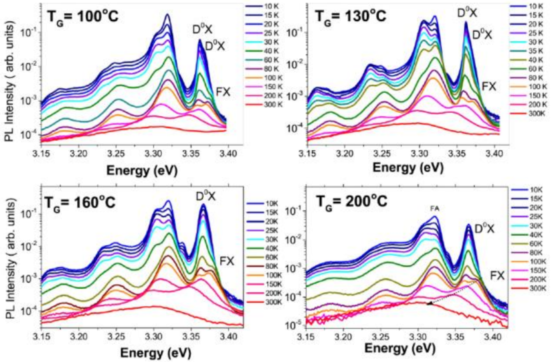
TEM measurements
Piotr Dłużewski, IF PAN



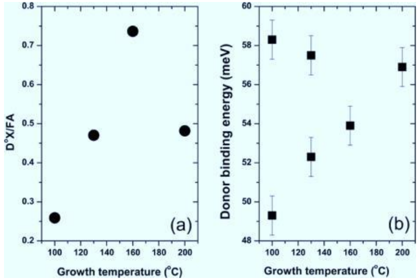




E. Przezdziecka, E. Guziewicz, D. Jarosz, et al., **J. Applied Physics** (2021)

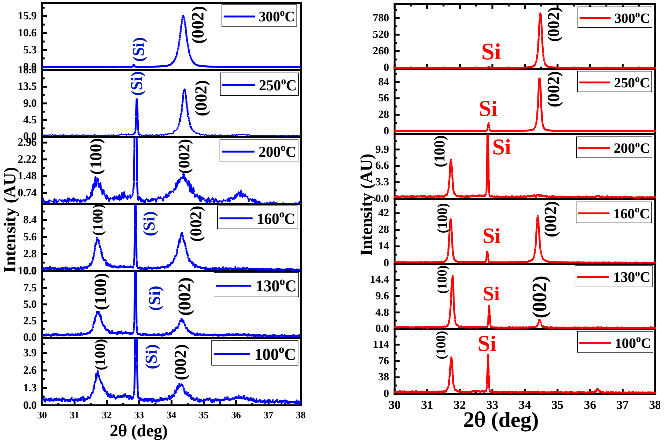


D°X /FA peaks at 10 K

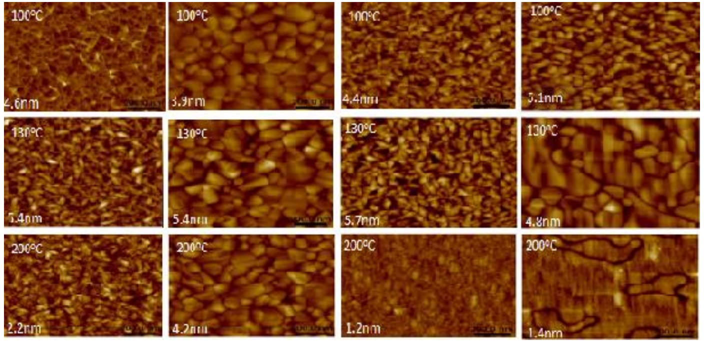


E. Guziewicz, **Oxide-based Materials and Structures: Fundamentals and Applications**, 2020 Taylor & Francis Group, LLC Corp. (2020) (pp. 201-228) Chapter 8 *Zinc Oxide Grown by Atomic Layer Deposition: A Versatile Material for Microelectronics*

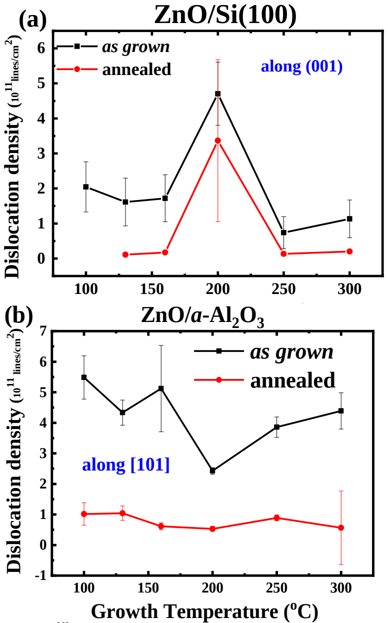
ZnO/Si and ZnO/Al_2O_3 by ALD

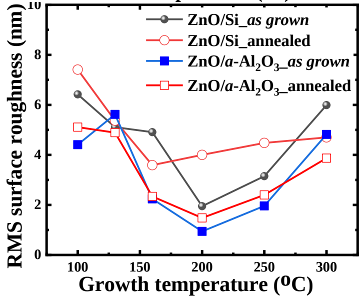


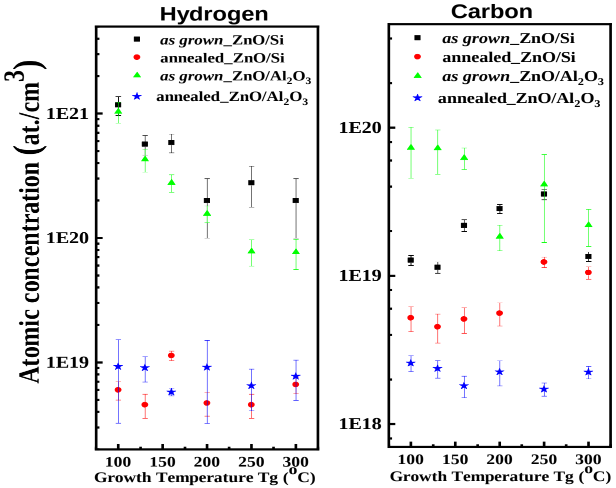
as grown annealed as grown annealed



ZnO/Si (100) ZnO/a-Al_2O_3





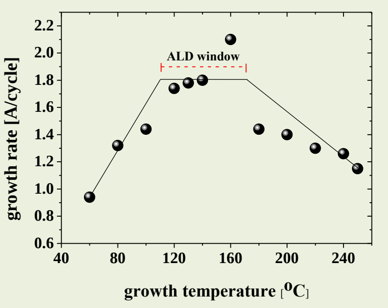


- Carriers' transport via GB-scattering route (except RTP ZnO/Si). Not only the H content (similar in both series) also growth conditions determine the conductivity of ZnO

- ZnO/Si(100) showed much lower structural defects compared to ZnO/a-Al_2O_3 and lower carrier concentration after 3 min.

Mishra et al., Materials, 14, p.4048 (2021)

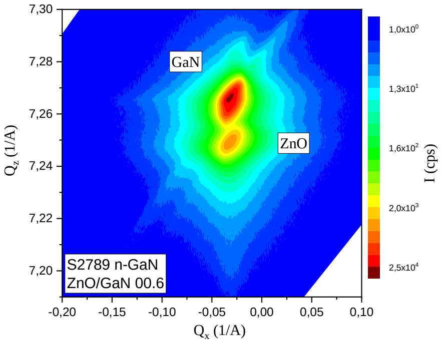
ZnO by ALD – epitaxial growth

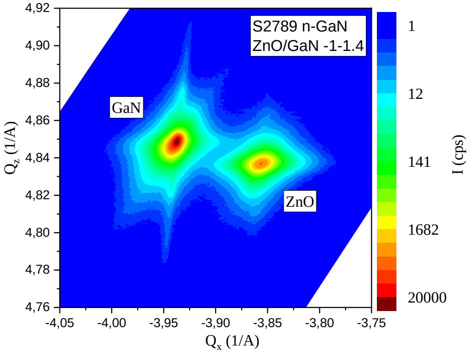


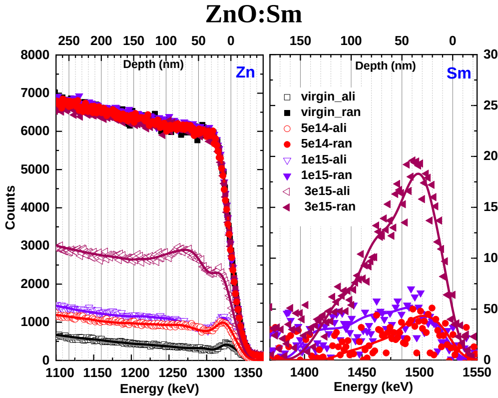
$T_G = 300°C$

$Zn(C_2H_5)_2 + H_2O \rightarrow ZnO + 2C_2H_6$

XRD - A. Wierzbicka







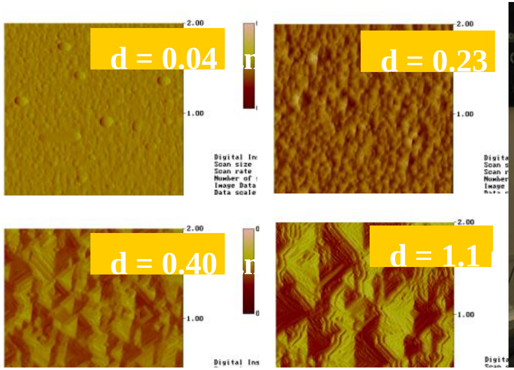
Epitaxial ZnO films – quality appropriate for RBS study (chi$_{min}$ ~ 3%) and RE implantation

- *T.A. Krajewski, R. Ratajczak, S. Kobyakov, W. Wozniak, K. Kopalko, E. Guziewicz,* ***Mat. Sci. Eng. B 275*** *(2022) 115526*
- *M. Sarwar, R. Ratajczak, V. Yu. Ivanov, S. Mishra, M. Turek, A. Wierzbicka, W. Wozniak, E. Guziewicz,* ***Adv. Sci.Technol. Res. J. 16(5)****, 147-154 (2022)*

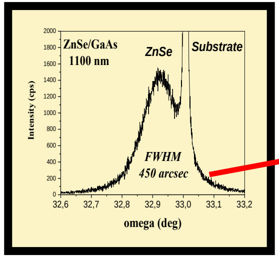
ZnSe films for TFEL displays

- Precursors (reactants): elemental Zn and Se

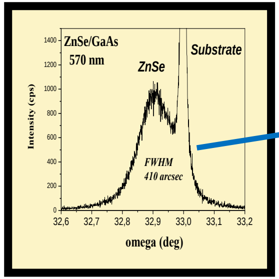
  Zn + Se → ZnSe
- Substrate: GaAs(100) n-type
- Growth temperature 430°C; epitaxial growth (XRD)



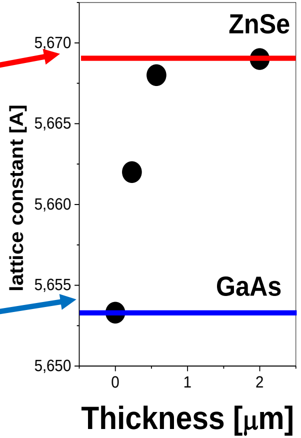
Atomic Force Microscopy (AFM) → ordered surface with pyramidal pits of the same orientation

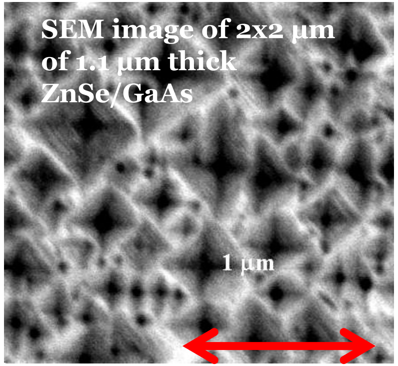


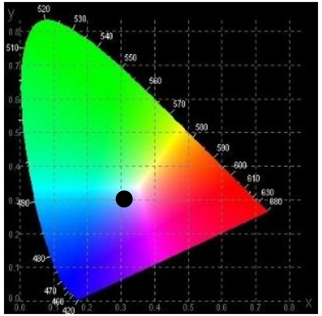
1.1 µm

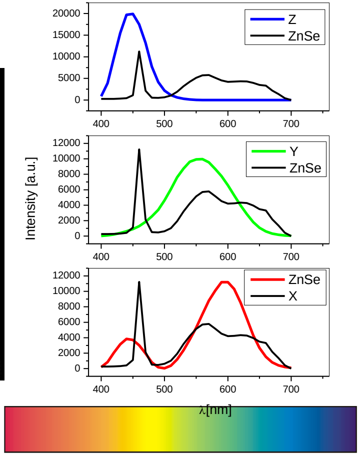


570 nm









Result → Mixing of ZnSe/GaAs PL bands give white color light

Ternary alloys and doping

Conductive AZO films

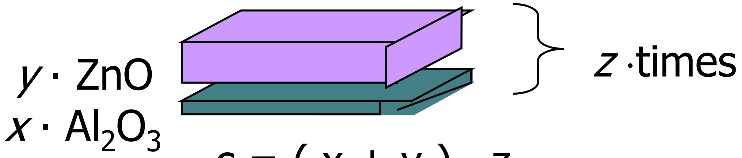
- AlZnO = AZO
- Al doping → Al precursor (Trimethylaluminum, TMA) introduced alternatively with Zn precursor (DEZn)

$$Zn(C_2H_5)_2 + H_2O \rightarrow ZnO + 2C_2H_6$$

$$2Al(CH_3)_3 + 3H_2O \rightarrow Al_2O_3 + 6CH_4$$

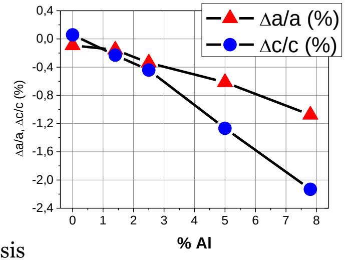
Al concentration: 0% - 8% (EDS)

$$c = (x + y) \cdot z$$

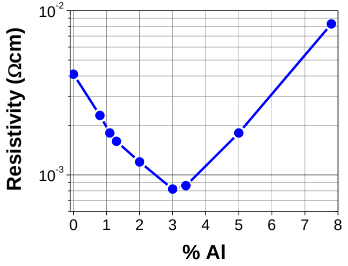


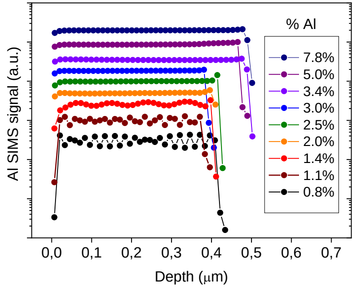
$$c = (x + y) \cdot z$$

XRD results: lattice parameters scales with Al content



G. Łuka, PhD thesis





SIMS results: uniform distribution of Al

High-k oxides

$$Hf[(CH_3)_2N]_4 + 2H_2O \rightarrow HfO_2 + 4HN(CH_3)_2$$

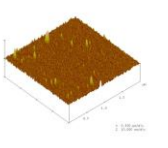
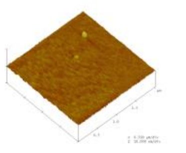
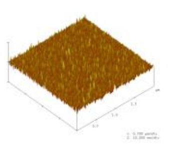
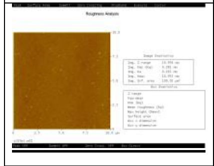
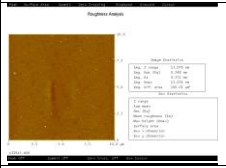
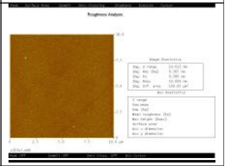
$$2Al(CH_3)_3 + 3H_2O \rightarrow Al_2O_3 + 6CH_4$$

Precursors:

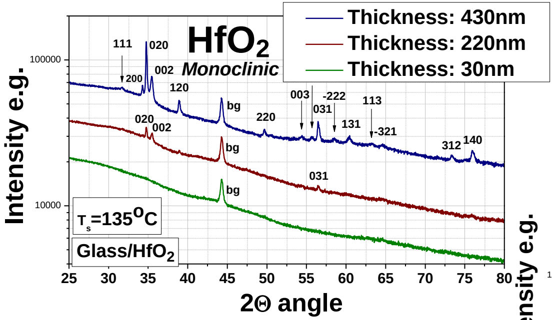
Oxygen– **H_2O** – deionized water;

Hafnium – **TDMAH** –tetrakis(dimetyloamido)hafnium(IV);

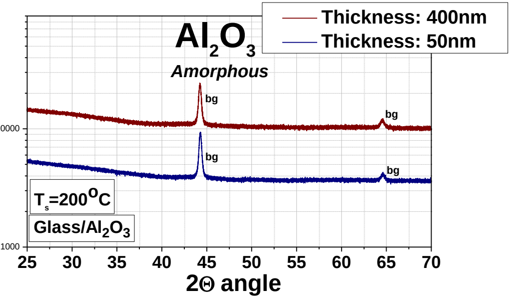
Aluminum – **TMA** –trimetylaluminum.

<table>
<tr><td colspan="3">c = 500</td></tr>
<tr><td colspan="3">TMA: 15 ms, H_2O: 15 ms</td></tr>
<tr><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td></td></tr>
<tr><td>T = 100°C
RMS: 0.281 nm</td><td>T = 200°C
RMS: 0.248 nm</td><td>T = 210°C
RMS: 0.365 nm</td></tr>
</table>

Porównanie wyglądu powierzchni z obrazów AFM próbek osadzanych przy parametrach procesu różniących się jedynie temperaturami osadzania warstw



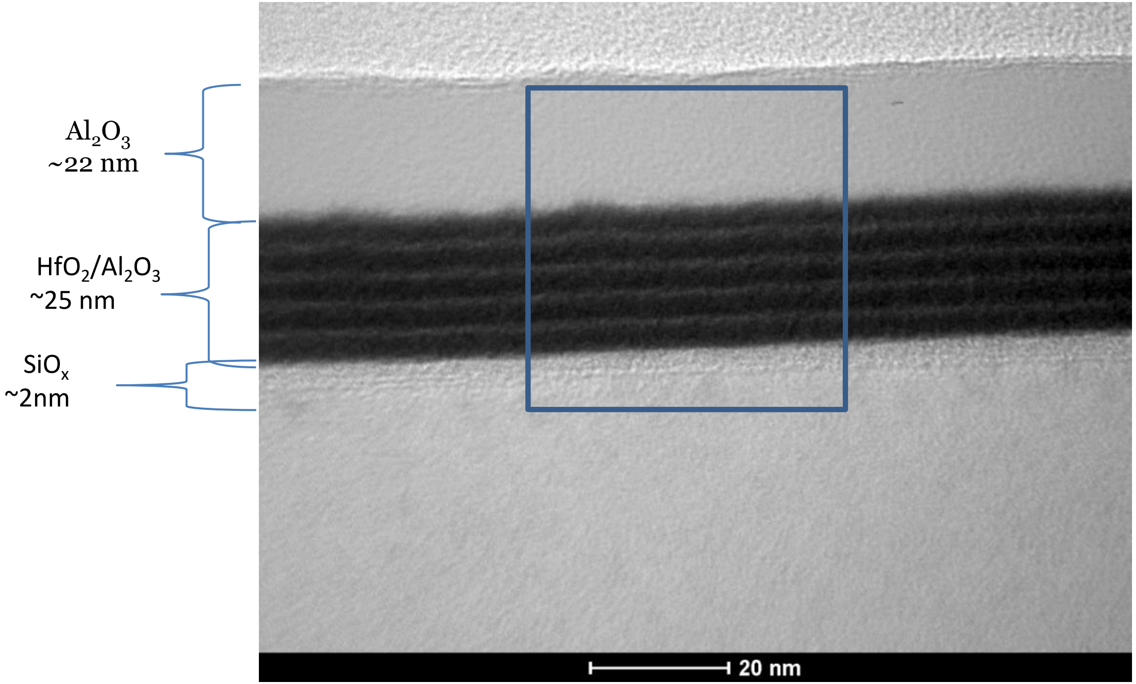
T_G = 60°C – 240°C



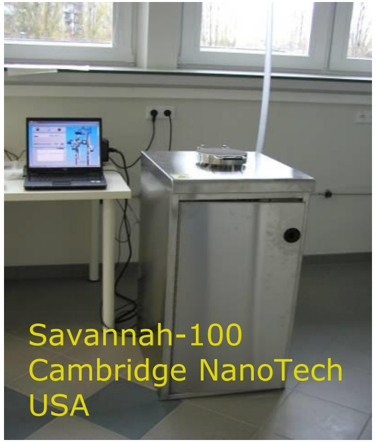
S. Gierałtowska, PhD thesis

Al_2O_3:HfO_2 composite layers - surface morphology

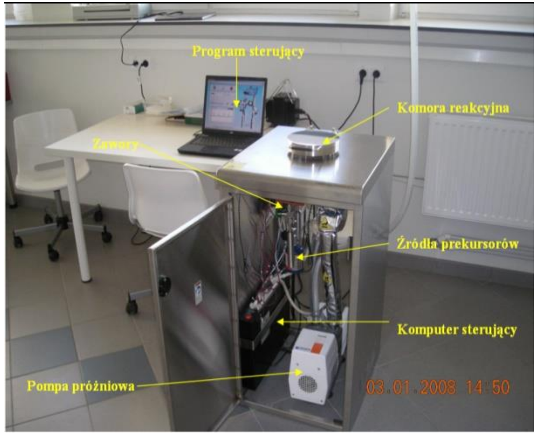
TEM BF

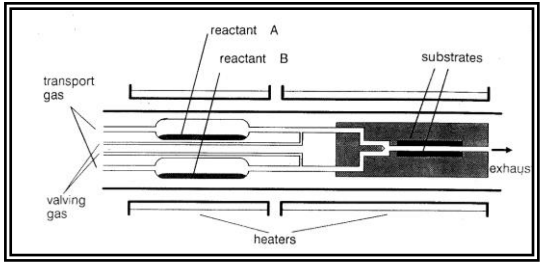


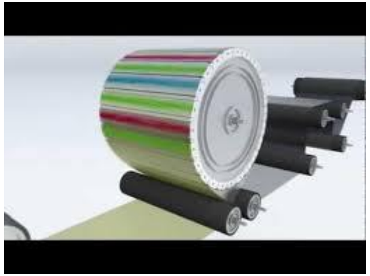
ALD reactors

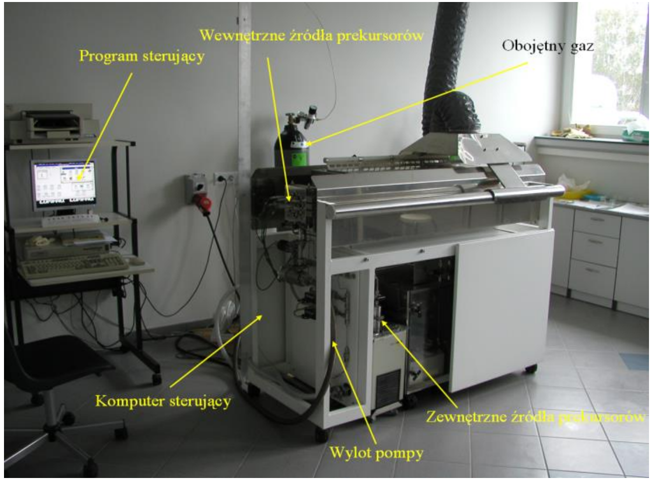


Savannah-100
Cambridge NanoTech
USA



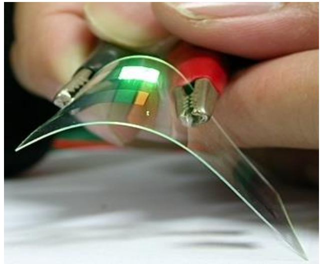


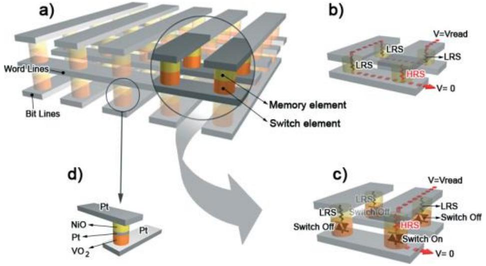


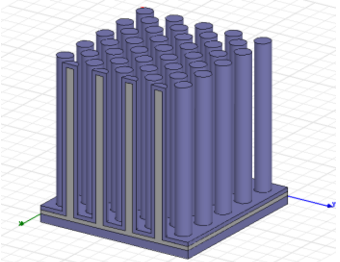


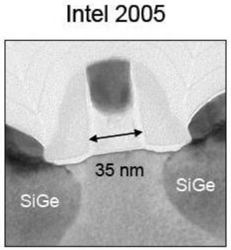
F-120, Microchemistry, Finland

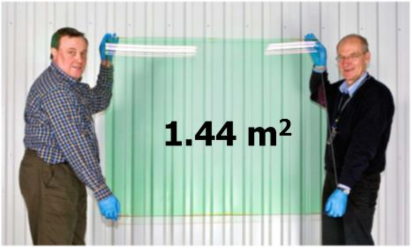
ALD → self-limiting growth











- Sequential deposition process:

- Precursors meet only on the surface, so can be more reactive than in Chemical Vapor Deposition (CVD) → possibility of **low deposition temperature** (3D memories, organic substrates)

- surface-related chemical reaction → possibility **to cover substrates of irregular shape** and highly developed morphology

- Self-limited growth process → for established ALD parameters (pulsing and purging times and temperature) thickness of the growing films scales with the number of ALD cycles (**thickness control in the nm scale**)

- Quality of growing films does not depend on spatial and temporal uniformity of precursors' flow (different than in case of CVD or MBE) → possibility to apply low volatility precursors**, possible large substrates**

- Possibility of using different reagents and different types of chemical reactions (synthesis, single or double chemical exchange) → **possibility to adjust the ALD process to our needs**

ALD applications and future

Last years we observe a booming interest in ALD, because:

- the prospective seen for ALD in scaling down microelectronic devices.
- ALD has proven essential to create gate dielectrics (materials: HfO2, ZrO2, Al2O3) on device substrates without native oxides, such as GaAs/AlGaAs heterostructures, organic transistors, nanotubes and many more.
- transition-metal nitrides (e.g. TiN, TaN, WN) for Cu interconnect barriers
- noble metals for ferroelectric random access memory (FRAM) and DRAM capacitor electrodes
- Cu interconnects and W plugs, or at least Cu seed layers for Cu electrodeposition and W seeds for W CVD